4a) Design and draw the omega network using 2x2 switch for the following:
   Input: 0 1 2 3 4 5 6 7 
   Output: 1 0 3 2 5 4 7 6 

b) Explain the basic structure of Tomasulo-based processor supports hardware speculation with a neat sketch.

5.a) What are functions of reservation stations? Explain the fields of reservation station in detail.

b) Explain the functions of branch prediction buffer in detail.

c) What are the decisions and transformations required for loop unrolling method?

6.a) For the given non-linear pipeline with reservation table given below:

   |   |   |   |   |   |   |
---|---|---|---|---|---|---|
0  | X | X | X | X | X | X |
1  | X | X |   |   |   |   |
2  |   |   |   |   |   |   |
3  |   |   |   |   |   |   |
4  |   |   |   |   |   |   |
5  |   |   |   |   |   |   |

   (i) Determine the forbidden latency, and initial collision vector
   (ii) Draw state transition diagram
   (iii) Determine Greedy cycles
   (iv) Determine Minimal average latency.

b) Explain the following instruction pipeline mechanisms:
   (i) Internal data forwarding. (ii) Hazard avoidance

7.a) Define the following with respect to pipelining:
   (i) Clock cycle (ii) Clock skew (iii) Efficiency (iv) Speedup factor (v) Throughput.

b) Explain how CDC scoreboard mechanism will increase the performance

c) Explain write invalidate cache coherence protocol with state diagram.

8a) Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential?

b) Explain Flynn's classification with a neat diagram.

c) Explain centralized shared memory architecture with a neat diagram.

d) Explain IEEE 754 floating point standard in detail.

9a) Explain advanced optimization of cache performance in detail.

b) Explain the internal architecture of DRAM with a neat sketch.

c) Explain the following:
   (i) Average memory access time (ii) Hit time (iii) Miss rate (iv) Miss penalty

10a) Explain the following with respect to scaling:
   (i) Bandwidth scaling (ii) latency scaling (iii) cost scaling (iv) physical scaling

b) Explain hardware parallelism and software parallelism in detail.
1.a) Consider the execution of object code with 2,00,000 instructions on 50 MHz processor. The program consists of 4 major types of instructions. The I mix & CPI needed for each is given below.

<table>
<thead>
<tr>
<th>I type</th>
<th>CPI</th>
<th>I mix</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arithmetic &amp; logic</td>
<td>1</td>
<td>60%</td>
</tr>
<tr>
<td>Load/store with cache</td>
<td>2</td>
<td>18%</td>
</tr>
<tr>
<td>branch</td>
<td>4</td>
<td>12%</td>
</tr>
<tr>
<td>Memory reference with cache miss</td>
<td>8</td>
<td>10%</td>
</tr>
</tbody>
</table>

Calculate CPI and Execution Time.

b) Explain Amdahl's law and also explain its factors.

c) What is computer architecture? Explain the dimensions of Instruction Set Architecture in detail.

OR

2.a) Explain the following computer classes:

i) Desktop
ii) Servers
iii) Embedded computers

b) Write the dependency graph for the following program statement.

```plaintext
S3: SUB RA, RB / RA <- RA - RB /
S4: MUL RA, 5 / RA <- RA * 5 /
S5: STORE M[20], RA / M[20] <- RA/
```

c) Explain the working of hypercube routing functions.

3.a) Explain how Bernstein’s conditions are used for detection of parallelism for the programming statements & also prove that parallelism consumes less time compare to Sequential processing.

P1: C = DXE
P2: M=G+C
P3: A=BXC
P4: C=L+M
P5: F= G/K

b) What is demand driven, control flow and data flow machine? Explain the differences between them in detail.