M.Tech SEMESTER END EXAMINATIONS – JUNE 2014

13LDE253 : ALGORITHMS FOR VLSI DESIGN AUTOMATION

NOTE: Answer any five full questions.

1.a) Explain the steps involved in reducing ordered BDDs. Draw the ROBDD for 3-input Ex-OR gate and 2-input And gate.
b) What is simulated annealing? Explain with the pseudo code, simulated annealing algorithm for partitioning.

2.a) Explain high-level synthesis using Y-chart and the hardware components used in high level synthesis system.
b) Define the “partitioning “of a VLSI design problem.
c) How do floor-planning and placement differ? Briefly explain the factors to be considered during floor planning and placement.

3.a) Explain the classification of placement algorithms.
b) Write the pseudo-code of Kernighan- Lin algorithm for partitioning. Apply the same and reduce the cut-size of the bisection given in figure.3 (b)

4.a) Mentioning the purpose of pin assignment, explain general pin assignment techniques.
b) Differentiate global and detailed routing.
c) Write and explain the program for Lee’s algorithm for routing.

5.a) Explain the placement process at system level, board level, and chip level. Briefly explain the cluster growth algorithm for placement.
b) How many 2-layer algorithms can be classified? Write left-edge algorithm for channel routing.

6.a) Explain the 4 classes of cell, models describing physical constraints for OTC routing.
b) Discuss the shadow propagation algorithm for one-dimensional compaction.
c) Briefly explain 2-dimensional compaction.
7.a) Define layout compaction. Mention the goals of compaction. Describe the 3-different ways to achieve these goals.

b) Explain the key ideas of over the cell routing using vacant terminals.

c) Discuss the classification of compaction algorithms.

8.a) Write short notes on
   i) Different stage of physical design cycle.
   ii) Constraint based floor planning
   iii) Simulated evolution technique.
   iv) Hierarchical compaction.